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## A low complexity joint equalizer and decoder for 1000Base-T Gigabit Ethernet

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### Abstract

A VLSI architecture for low complexity joint decoding and equalization for 1000Base-T Gigabit Ethernet is presented. A one-tap parallel decision-feedback decoder jointly decodes the trellis and cancels the first tap of the post-cursor channel impulse response. The one-dimensional branch metrics are precomputed in a look-ahead fashion to meet the speed requirements. The less significant tail of the impulse response is canceled with a simple decision-feedback prefilter. The design has been implemented in 0.25  $\mu\text{m}$  standard cell CMOS process for operation at 125 MHz.

### Index Terms

Inspe

#### Controlled Indexing

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### References

No references available on IEEE Xplore.

### Citing Documents

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